AMENDMENT

Unmarked Version

In the specification:

Please replace the following paragraphs:

- Page 10, paragraph starting at line 1 and ending at line 7:

The registers 141 represent a storage area on computer system 105 for storing information, such as control/status information, scalar and/or packed integer data, floating point data, etc. It is understood that one aspect of the invention is the described instruction set. According to this aspect of the invention, the storage area used for storing the data is not critical. The term data processing system is used herein to refer to any machine for processing data, including the computer system(s) described with reference to Figure 1.

- Page 10, paragraph starting at line 8 and ending at line 16:

Figure 2 illustrates one embodiment of the format of any one of the cache segment invalidate instructions 162, the cache segment flush instruction 164, and the cache segment flush and invalidate instructions 166 provided in accordance with the present invention. For discussion purposes, the instructions 162, 164 and 166 will be referred to as the cache control instruction 160. The cache control instruction 160 comprises and operational code (OP CODE) 210 which identifies the operation of the cache control instruction 160 and an operand 212 which specifies the name of a register of memory location which holds a starting address of the data object that the instruction 160 will be operating on.
